MEMORY SYSTEM

CI - 1123

TECHNICAL MANUAL

NOV 1981

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SECTION I

GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the elements of operation, installation, and design of the CI-1123 dynamic read/write memory.

1.2 THE MEMORY MODULE

The CI-1123 various options are summarized below:

OPTION	MEMORY CAPACITY	MEMORY CHIP UTILIZED
64K	64 K by 16 or 18 bits	64K by 1 (4164)
128K	128K by 16 or 18 bits	64K by 1 (4164)

1.2.1 CI-1123 MEMORY DESCRIPTION

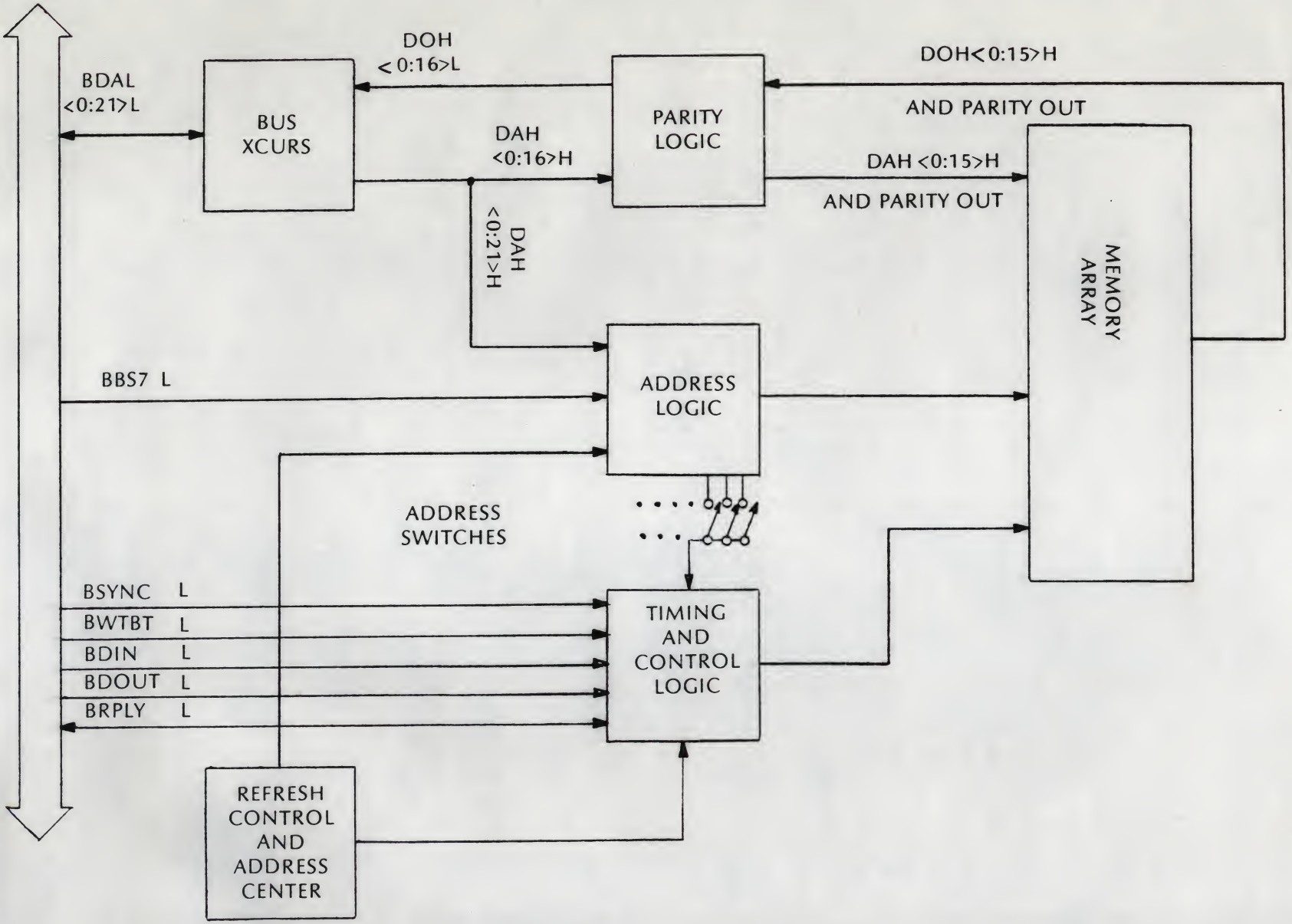
The CI-1123 is a high speed, high density dynamic read/write memroy which is plug compatible with the DEC LSI 11/2, LSI 11/23, PDP-1103, and PDP-1123. Memory storage is provided by 64K by 1 dynamic MOS memory chips. The memory is a single package plug-in module having dimensions of 8.44" x 5.187".

1.2.2 OPERATIONAL FEATURES

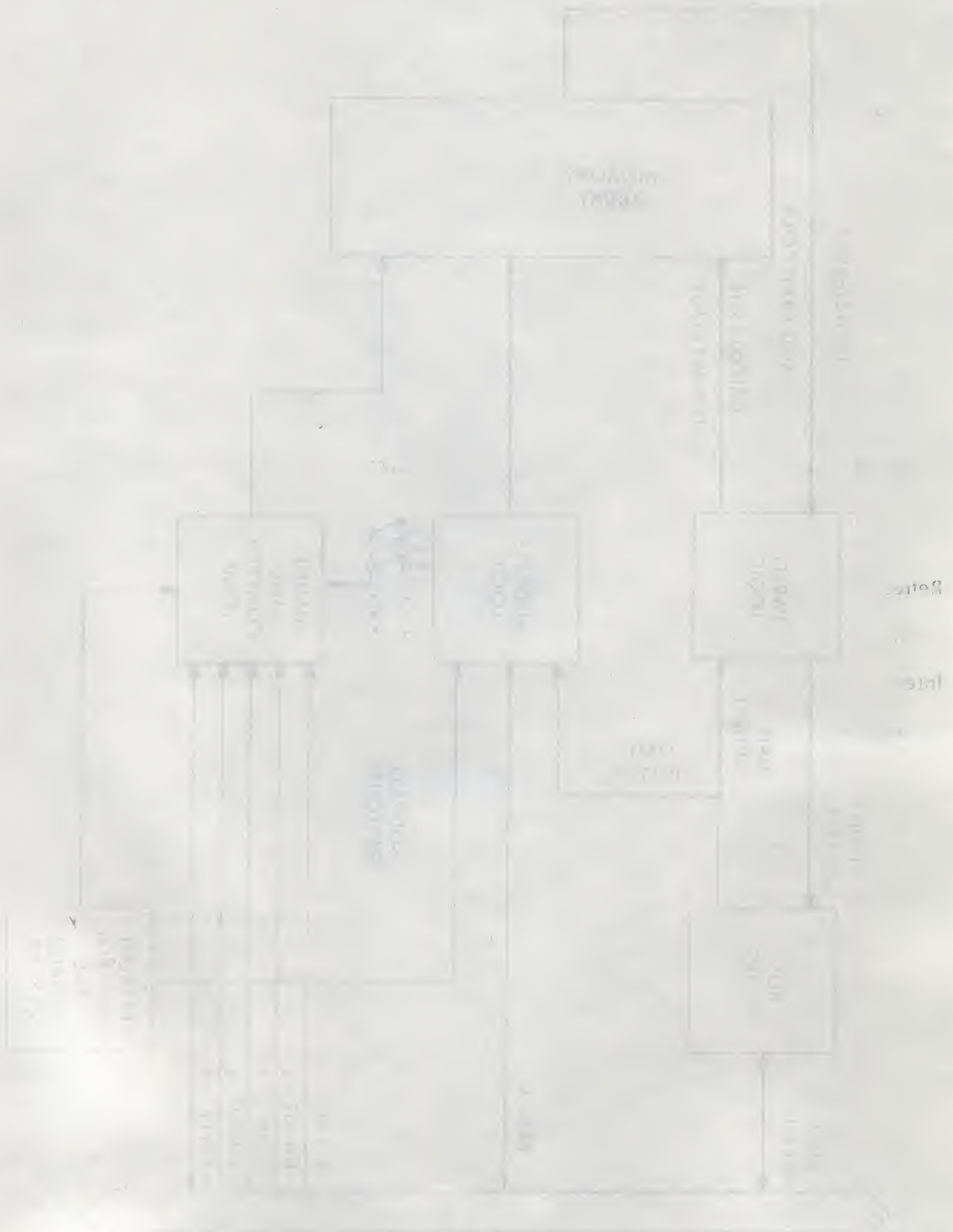
The memory module contains its own address and data buffers. Address, data-in and data-out are multiplexed for bus compatibility with the Q-Bus. The system memory address space to which the module will respond is user-configured via switches contained on the module. An address can be selected in 4K increments through the 0-4 Megabyte address range. The module contains its own complete refresh control logic requiring no outside intervention. The module generates and checks even parity which is totally DEC hardware and software compatible.

1.2.4 POWER REQUIREMENTS

The memory module requires a single power source supplied by the system 5 volt supply.



FUNCTIONAL BLOCK DIAGRAM
FIGURE 1.1



1.3 GENERAL SPECIFICATION REQUIREMENTS

Table 1.3.1 lists the general specifications for the CI-1123 memory.

TABLE 1.3.1

CHARACTERISTICS	SPECIFICATIONS
Capacity	64KW to 128KW x 16 or 18 bits
Cycle Time	400 nanoseconds
Access Time	240 nanoseconds from sync active
Word Size	16 bits
Address	22 bits (random access)
Data-in/Data-out	16 bits bidirectional with open collector TTL voltage compatible
Modes of Operation	DATO, DATOB, DATI, DATIO, DATIOB
Expansion	4KW Memory Blocks up to 4 Megabyte by selecting the proper switch
Refresh	On Board distributed
Parity	Even
Interface Signals	
Inputs	TTL Compatible
Outputs	Open Collector
Operating Temperature	0 to 60 DEG C
Storage Temperature	-20 to 70 DEG C

Power Requirements

MODE	NORMAL		BACKUP	
	Operate	Standby	Operate	Standby
+5.0V	1.4A	1A	700mA	---
+5VB	---	---	700mA	300mA

Dimensions	8.44" x 5.187"

1.4 MEMORY ADDRESS SELECTION

(Refer to drawing 70754 for switch and PEG location)

1.4.1 OPTION 1 - 4K WORD INCREMENT SELECTION

The CI-1123 128K is shipped in OPTION 1 configuration. In this configuration the placement of PEG in AREA A enables the entire lower 64KW of memory (000000 to 377777, PEG between posts 2 and 3) or the entire upper 64KW of memory (400000 to 777777, PEG between posts 1 and 2). The remaining portion of memory is selected in 4KW increments by closing the appropriate switches per table 1.4.1.

TABLE 1.4.1

BANK SELECTED AREA A PEG POSITION 1 - 2	BANK SELECTED AREA A PEG POSITION 2 - 3	CLOSED SWITCH (on)	BANK SELECTED AREA B PEG POSITION 1 - 2	BANK SELECTED AREA B PEG POSITION 2 - 3	CLOSED SWITCH (on)
000000 to 017777	400000 to 417777	SW1-1	200000 to 217777	600000 to 617777	SW2-1
020000 to 037777	420000 to 437777	SW1-2	220000 to 237777	620000 to 637777	SW2-2
040000 to 057777	440000 to 457777	SW1-3	240000 to 257777	640000 to 657777	SW2-3
060000 to 077777	460000 to 477777	SW1-4	260000 to 277777	660000 to 677777	SW2-4
100000 to 117777	500000 to 517777	SW1-5	300000 to 317777	700000 to 717777	SW2-5
120000 to 137777	520000 to 537777	SW1-6	320000 to 337777	720000 to 737777	SW2-6
140000 to 157777	540000 to 557777	SW1-7	340000 to 357777	740000 to 757777	SW2-7
160000 to 177777	560000 to 577777	SW1-8	360000 to 377777	760000 to 777777	SW2-8

NOTE: For full 128K memory implementation all switches should be closed.

OPTION 2 - 8K WORD INCREMENT SELECTION

The CI-1123 64K is shipped in OPTION 2 configuration. In this configuration PEG in AREA A is placed between posts 2 and 4. The memory is selected in 8KW increments by closing the appropriate switches per table 1.4.2.

TABLE 1.4.2

BANK SELECTED	CLOSED SWITCH	BANK SELECTED	CLOSED SWITCH
000000 to 037777	SW1-1	400000 to 437777	SW2-1
040000 to 077777	SW1-2	440000 to 477777	SW2-2
100000 to 137777	SW1-3	500000 to 537777	SW2-3
140000 to 177777	SW1-4	540000 to 577777	SW2-4
200000 to 237777	SW1-5	600000 to 637777	SW2-5
240000 to 277777	SW1-6	640000 to 677777	SW2-6
300000 to 337777	SW1-7	700000 to 737777	SW2-7
340000 to 377777	SW1-8	740000 To 777777	SW2-8

NOTES: 1. On the CI-1123 64K a total of 8 switches can be closed, and the memory field selected should be contiguous.

2. See APPENDIX A for reconfiguration from memory select OPTION 1 to memory select OPTION 2.

1.4.3 BANK 7 SELECTION OPTION

The CI-1123 is disabled whenever the BBS7L Signal is asserted on the bus. The lower 2K portion of BANK 7 can enabled by moving PEG in AREA B from posts 2 and 3 to posts 1 and 2.

NOTE: User must take caution to insure no I/O devices utilize the lower 2KW portion of BANK 7 or bus contention will occur resulting in inproper system operation.

1.4.4 EXTENDED MEMORY SELECTION TO 4 MEGABTES

For extended memory selection implementation see APPENDIX A.

SECTION II

HANDLING AND INSTALLATION

2.1 INTRODUCTION

This section details handling precautions. It includes step by step procedures to interface the CI-1123 memory with the LSI-11/23 and the PDP-1123 microcomputer family.

2.2 HANDLING PRECAUTIONS

The memory IC's used on the CI-1123 are MOS devices. They can be damaged by static electricity discharge. Always handle MOS IC's so that no discharge will flow through the IC. Also avoid unnecessary handling and wear cotton--rather than synthetic--clothing when you do handle these IC's.

2.3 INTERFACE SIGNALS

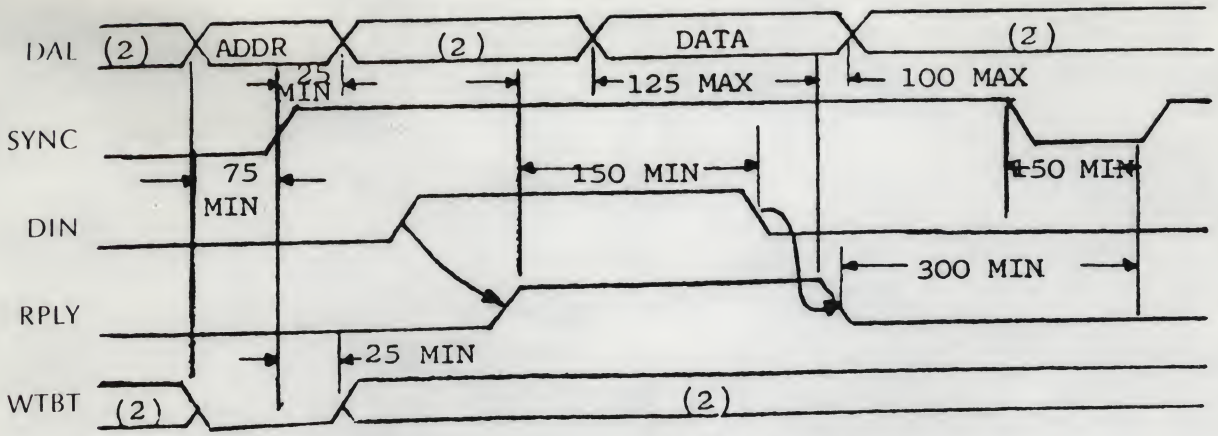
The input signals to the memory are TTL compatible and the output signals are open collector. The timing relationship between these signals are shown in figure 2.1.

2.4 INTERFACE WITH THE LSI 11/23 OR PDP-1123

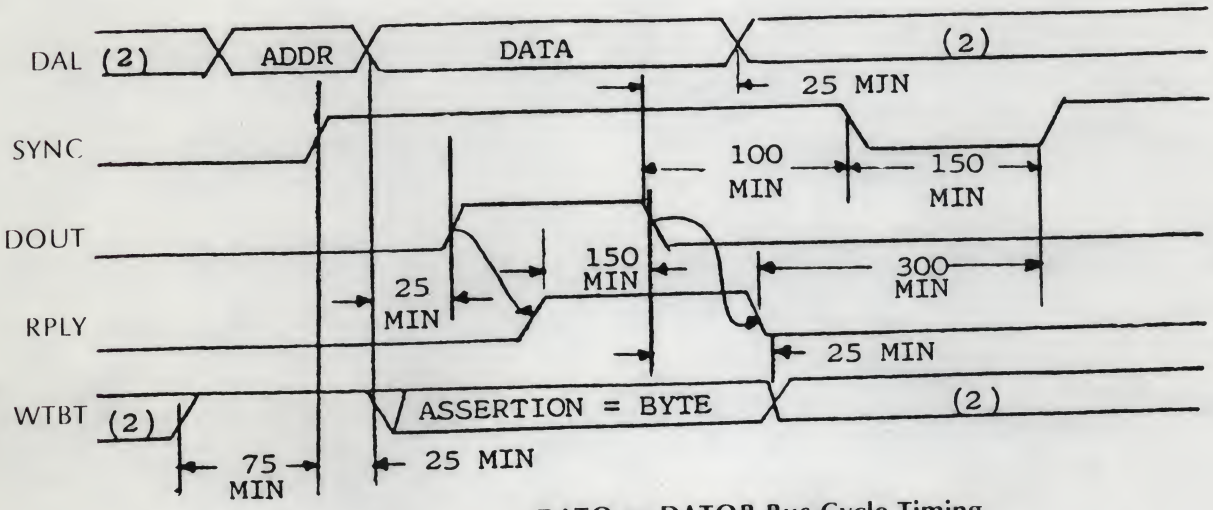
The CI-1123 memory module may be installed in any slot available in the PDP-1123.

CAUTION: The memory module and backplane connector can be damaged if the module is installed backwards. Care should be taken to insure that the module is installed so that the component side of the module faces the same direction as other LSI-11 modules.

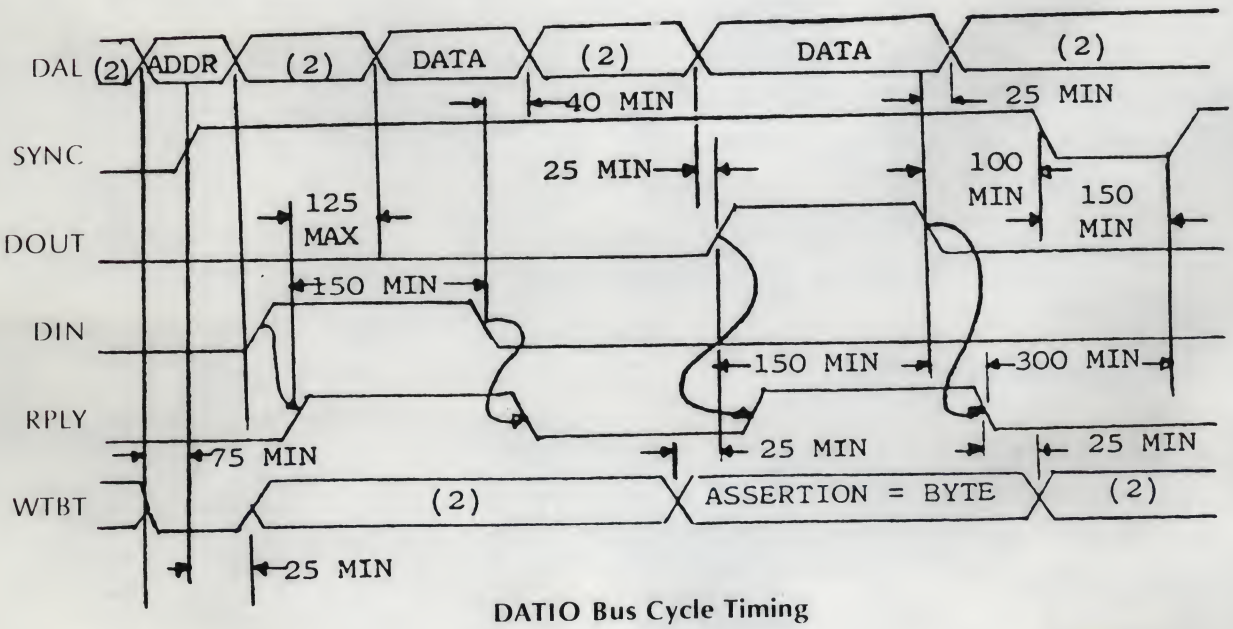
DC power must be removed from the backplane during module removal or insertion.



DATI Bus Cycle Timing



DATO or DATOB Bus Cycle Timing



DATIO Bus Cycle Timing

1. All timing signals in Nano Seconds (ns).
2. Don't care condition.

MEMORY INTERFACE DIAGRAM
FIGURE 2.1

CONNECTOR PIN ASSIGNMENT

SIGNAL NAME	COMP. SIDE	SOLDER SIDE	SOLDER SIDE
	AA1	AA2	+5V
	AB1	AB2	
BDAL16L	AC1	AC2	GND
BDAL17L	AD1	AD2	
	AE1	AE2	BDOUTL
	AF1	AF2	BRPLYL
	AH1	AH2	BDINL
GND	AJ1	AJ2	BSYNCL
	AK1	AK2	BWTBTL
	AL1	AL2	
GND	AM1	AM2	BIAKIL
	AN1	AN2	BIAKOL
	AP1	AP2	BBS7L
	AR1	AR2	BDMGIL
	AS1	AS2	BDMGOL
GND	AT1	AT2	
	AU1	AU2	BDALOL
+5B	AV1	AV2	BDALIL
BDCOKH	BA1	BA2	+5V
	BB1	BB2	
BDAL18L	BC1	BC2	GND
BDAL19L	BD1	BD2	
BDAL20L	BE1	BE2	BDAL2L
BDAL21L	BF1	BF2	BDAL3L
	BH1	BH2	BDAL4L
GND	BJ1	BJ2	BDAL5L
	BK1	BK2	BDAL6L
	BL1	BL2	BDAL7L
	BM1	BM2	BDAL8L
	BN1	BN2	BDAL9L
	BP1	BP2	BDAL10L
	BR1	BR2	BDAL11L
	BS1	BS2	BDAL12L
GND	BT1	BT2	BDAL13L
	BU1	BU2	BDAL14L
+5	BV1	BV2	BDAL15L

TABLE 2-1

SECTION III

THEORY OF OPERATION

3.1 GENERAL DESCRIPTION

A memory module is the portion of a computer system where data is stored or retrieved at full processor speed. The process of storing or retrieving a data word or byte is known as a memory access.

A cycle is a series of events resulting in one memory access. The CI-1123 performs six kinds of cycles: DATI, DATO, DATOB, DATIO, DATIOB, and REFRESH.

3.1.1 CYCLES OTHER THAN REFRESH

Cycles other than refresh are termed memory cycles. There are five kinds of memory cycles described as follows:

DATI: This cycle performs one 16 bit word read operation from the generated bus address.

DATO: This cycle performs one 16 bit word write operation to the generated bus address.

DATOB: This cycle performs one 8 bit byte write operation to the generated bus address.

DATIO: This cycle is termed as a read-modify-write cycle. It performs a 16 bit read operation from the generated bus address followed by a 16 bit write operation to the same address.

DATIOB: This cycle is the same as DATIO except the operation is on an eight bit byte instead of a 16 bit word.

All memory cycles are initiated in the same manner on the CI-1123 memory module. If the generated bus address is one selected according to the memory address selection configuration (section 1.4), a board select signal occurs (BS). The memory cycle then begins on the falling edge of PSYNCL (AJ2). Module control and decode logic selects the specific internal memory location. At this point various control inputs from the Q BUS determine which one of the five kinds of memory cycles will be performed.

3.1.2 REFRESH CYCLES

A refresh cycle is an internally generated and controlled memory access performed to insure the integrity of the stored data. Refresh cycles are performed on a regulated periodic basis and are interleaved between memory cycles. A refresh cycle can be thought of as a dummy read cycle.

* 3.2 DETAILED DESCRIPTION

3.2.1 BOARD SELECTION

Page and board selection depends on latched address bits A12-A21, three decoders, U15, U21, U22, and the two 8 position switches SW1 and SW2.

Latched address bits A17 (U12-2) and $\overline{A17}$ (U19-2) are applied to a portion of U4 to determine the page selected. This allows the RAS Strobe (U7-10) to be applied only to that group of memory chips.

Latched address bits A13-A16 are applied to decoders U15 and U22 with open collector outputs. These outputs are wired "OR" via the two eight position switches (SW1 and SW2) to determine the board select condition. Switch position "1" on SW1 enables the 1st 4KW bank and succeeding switch positions enable the remaining 4KW banks thru 64KW. The A17 or $\overline{A17}$ signal is also fed into the wired "OR" signal via U20-2 and peg setting in Area A. This allows the wired "OR" signal to be low for the first 64KW of memory (A17 jumpered to U21-1) or the second 64KW of memory (A17 jumpered to U21-1).

If the wired "OR" signal is low and DISABLE (U23-6) is low the BOARD SELECT signal (BS U24-4) becomes true (high). DISABLE becomes true (high) for any one of two reasons. First, if BBS7L is active meaning an I/O operation is to be performed. Second, if the bus address generated is for a 256K byte bank other than the bank select thru U21 and jumper Area C according to Appendix A.

If BS is true the falling edge of PSYNCL will initiate a memory cycle thru part of U16.

3.2.2 CYCLES

Either of two signals $\overline{MC}$ or $\overline{RC}$ can initiate a cycle. $\overline{RC}$ describes a refresh cycle and $\overline{MC}$ describes any of the LSI-11 memory cycles.

$\overline{MC}$ and $\overline{RC}$ are OR'ed in U6, with the output on pin 6 being applied to DL1. DL1 is a passive delay line producing all the required timing for address strobes and enables to memory.

3.2.2.1 DATI CYCLE (REFER TO FIG. 3.1)

This cycle retrieves data from the indicated address. If board select (BS U24-4) is true the rising edge of SYNC RC (U24-10) clocks flip/flop U16 which sets the MC signal starting a cycle thru DL1. $\overline{RAS}$ occurs at the selected page of memory causing the Row Address to be saved, and starting a cycle within each of the eighteen memory IC's.

After 25nsec CAE (Column Address Enable, U7-6) becomes active disabling the Row Address (Octal Latch U13) and enabling the Column Address (Octal Latch U14) to be present to the memory array.

After 75nsec, CAS (Column Address Strobe U24-13) is set. $\overline{CAS}$ occurs at all memory IC's. Within the eighteen IC's selected by $\overline{RAS}$ the column address is saved. This is a read cycle therefore $\overline{WR0}$ and $\overline{WR1}$ are high and the input data is ignored.

After 150nsec, the reply logic is enabled (U17-5). Once BDINL becomes active $\overline{DOE}$ (Data Out Enable U18-6) occurs allowing the bus transcievers to drive the Q-bus with valid data from the Memory Array. $\overline{DOE}$ in turn generates BRPLY L.

Once PSYNCL is removed, MC will reset terminating the cycle in process.

3.2.2.2 DATO CYCLE (REFER TO FIGURE 3.2)

This cycle stores data at the indicated address. The cycle proceeds much the same as a DATI cycle except that a BDOUTL occurs instead of BDINL. This is not a DATOB cycle therefore BWTBTL is not asserted. Valid new data reaches the Memory Array via the bus transceivers U25 thru U29. BDOUTL occurs which along with RPLY EN (U17-5) results in $\overline{WR0}$ and $\overline{WR1}$ becoming active. Write strobes $\overline{WR0}$ and $\overline{WR1}$ store the new data at the selected address. BRBLYL is generated and the cycle is terminated as in a DATI cycle.

3.2.2.3 DATOB CYCLE (REFER TO FIGURE 3.2)

This cycle proceeds the same as a DATO cycle except BWTBTL is asserted indicating the cycle is a write byte only. AO (U12-6) and U23 determine whether the lower or upper byte is written into allowing only $\overline{WR1}$ or $\overline{WR0}$ to become active.

3.2.2.4 DATIO OR DATIOB (REFER TO FIGURE 3.3)

This cycle performs a read followed by a write or write byte operation. The first portion of the cycle proceeds as a normal DATI cycle. Once the DATI portion is completed BSYNCL remains active and therefore the $\overline{RAS}$ signal to the selected page remains active. At this time data is placed on the bus and BDOUTL is asserted as in a DATO cycle resulting in DATA being written into the selected address location. BWTBTL determines the write byte condition as before and AO determines the lower or upper byte.

3.2.2.5 REFRESH CYCLE (REFER TO FIGURE 3.4)

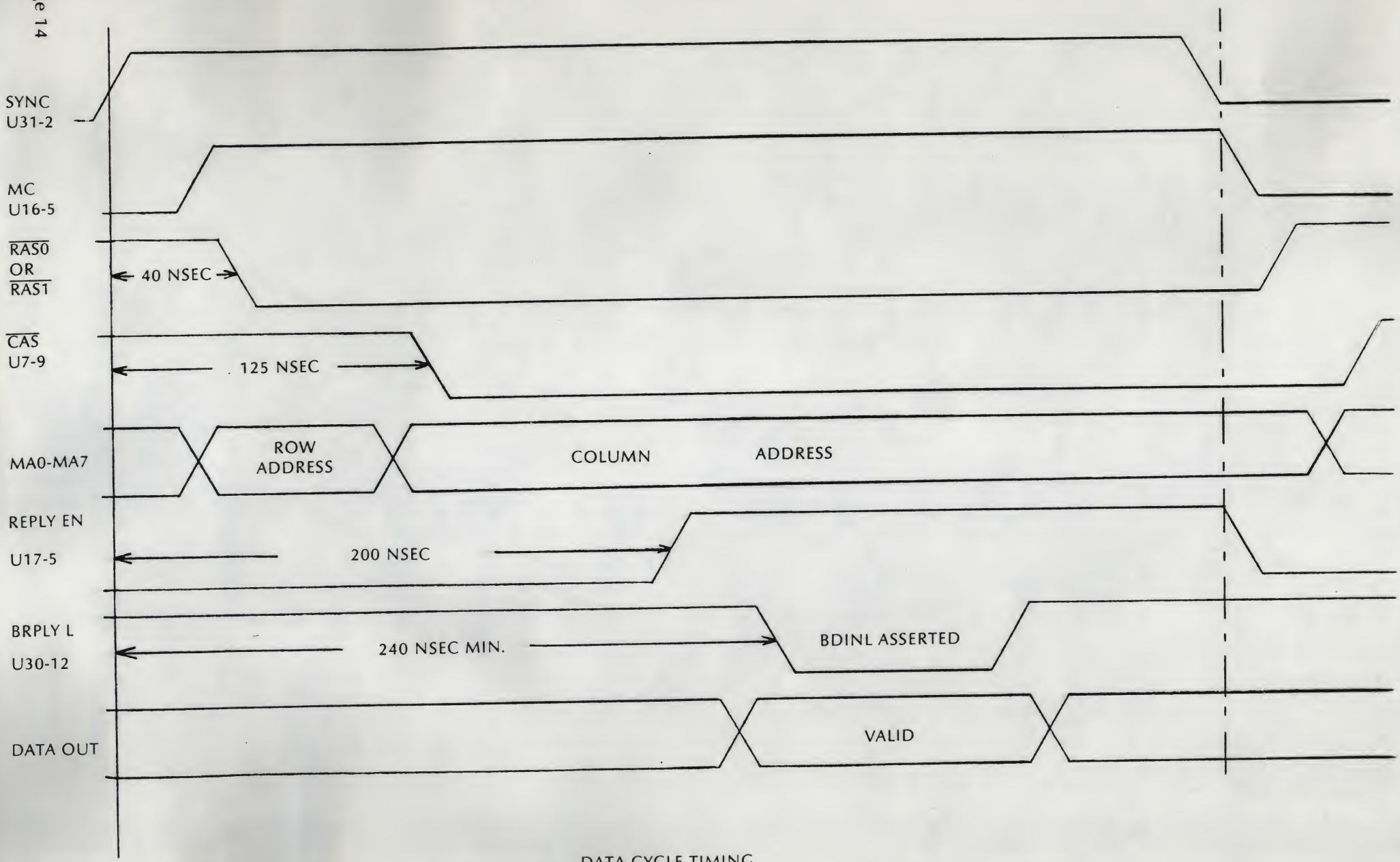
This cycle refreshes data in one Row in each memory IC when it occurs.

The CI-1123 controls the refreshing of memory itself requiring no outside intervention. This is accomplished thru the use of the 8 bit counter U2 and one shot U32. One part of U32 times out a 12 micro second interval at which time a refresh cycle is requested. If no cycle is in progress and the system is in a non-active sync period, the request is granted. REF CY (U17-9) is set enabling the counter address to reach the Memory Array via multiplexers U1 and U3. REF CY generates a 225nsec strobe through the other part of U32 which is applied to the delay line as the RC signal (U32-4). RAS becomes active as in other cycles, but because REF CY is active RAS occurs at both pages of memory. The Row Address is strobed resulting in one of 128 Row locations being refreshed. The CAS signal is disabled and no further strobing of the memory array occurs. 75nsec after the termination of the RC signal flip/flop U17 is clocked clearing REF CY allowing other cycles to occur.

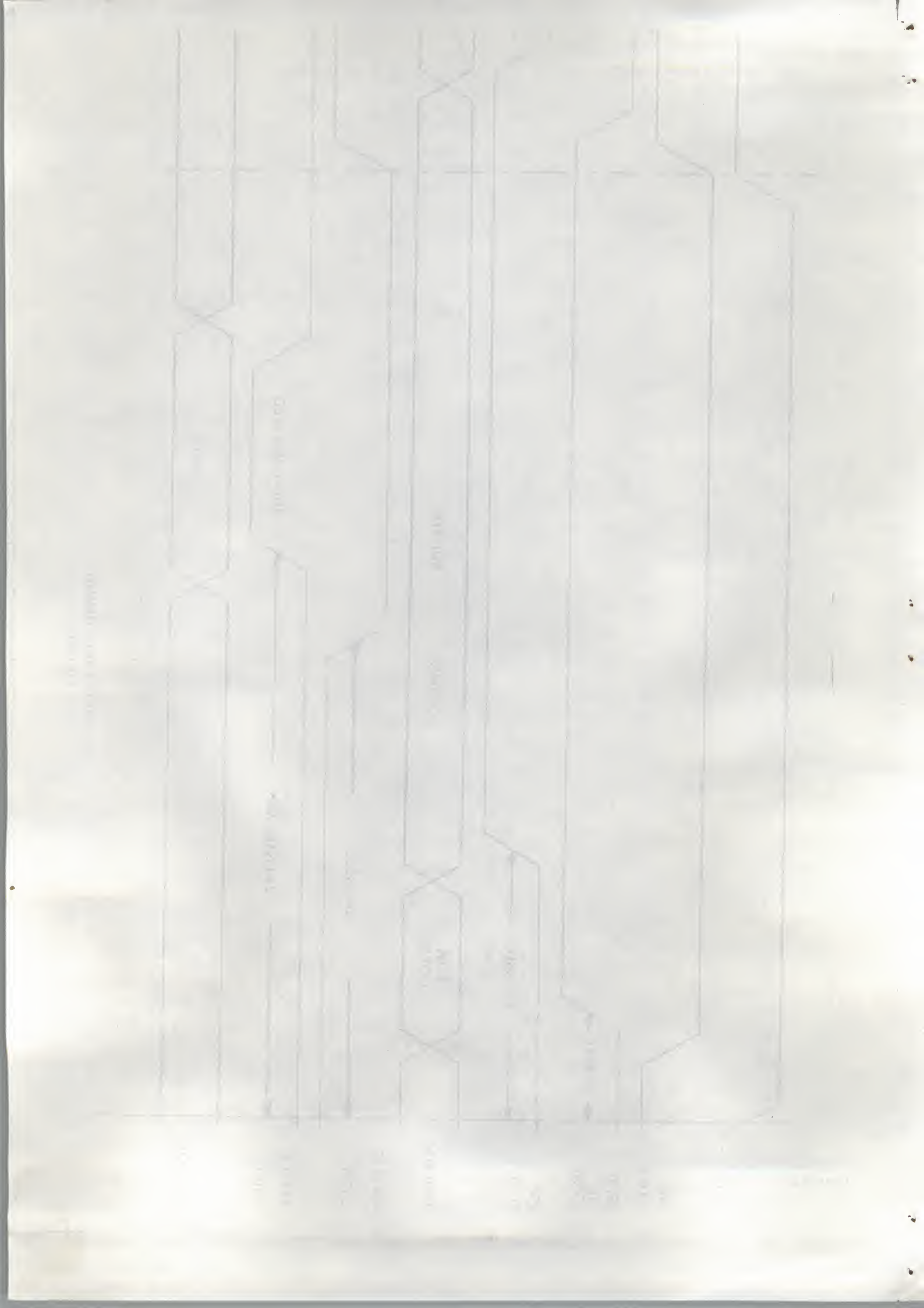
3.2.3 PARITY LOGIC

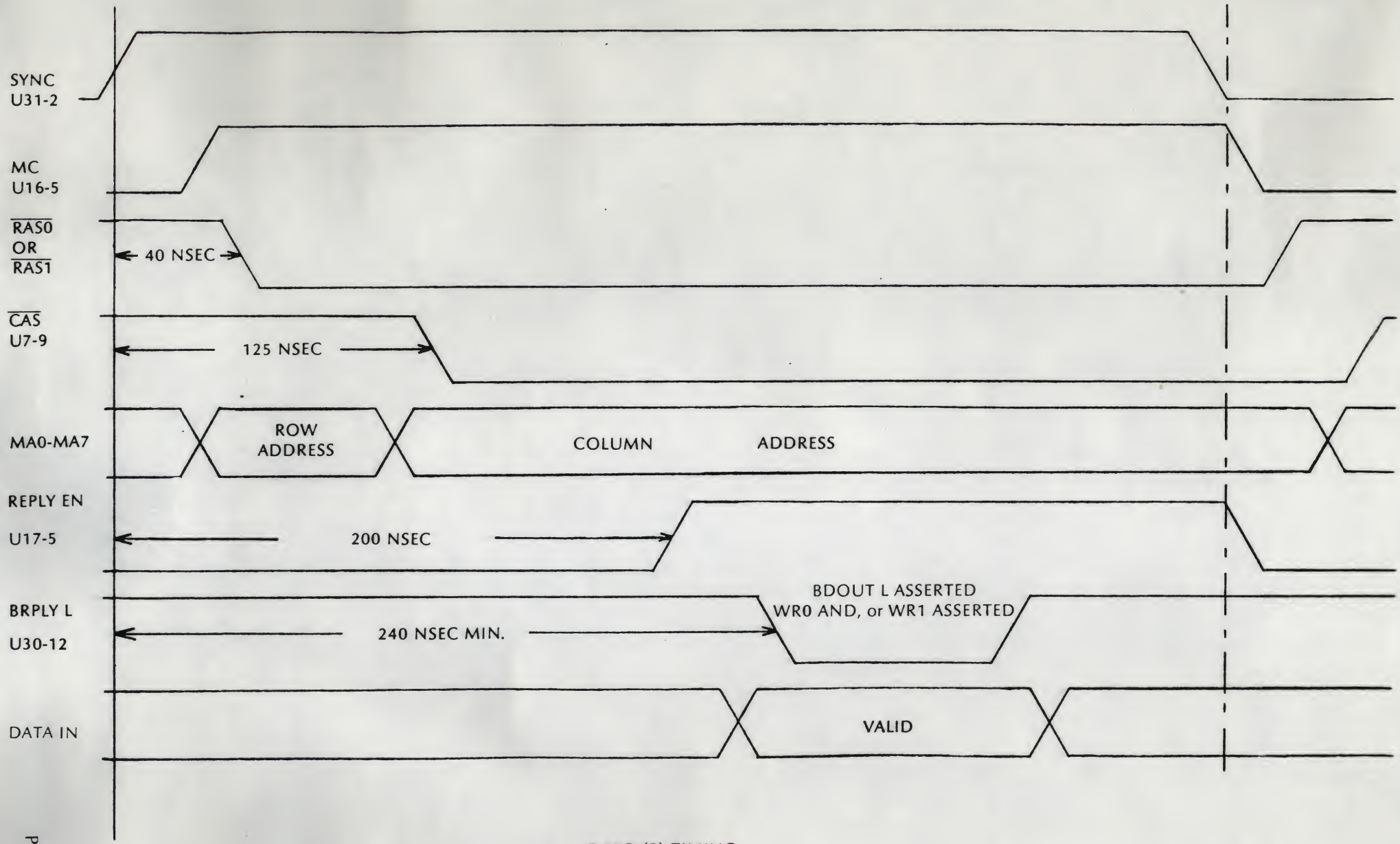
Parity logic consists of four parity generator checkers U8 through U11, flip/flop U16 and associated logic circuitry. Parity is checked on all memory read cycles. If a parity error occurs U24-1 will be low when the reply logic is enabled. The reply logic generates a clock to the Parity Error Flip/Flop setting PE (U16-8). The active PE signal drives BDAL16 L during read operations indicating a parity error to the system.

Timing specified in this section is based on set values generated thru DL-1, therefore propagation delays must be considered for actual measurements.

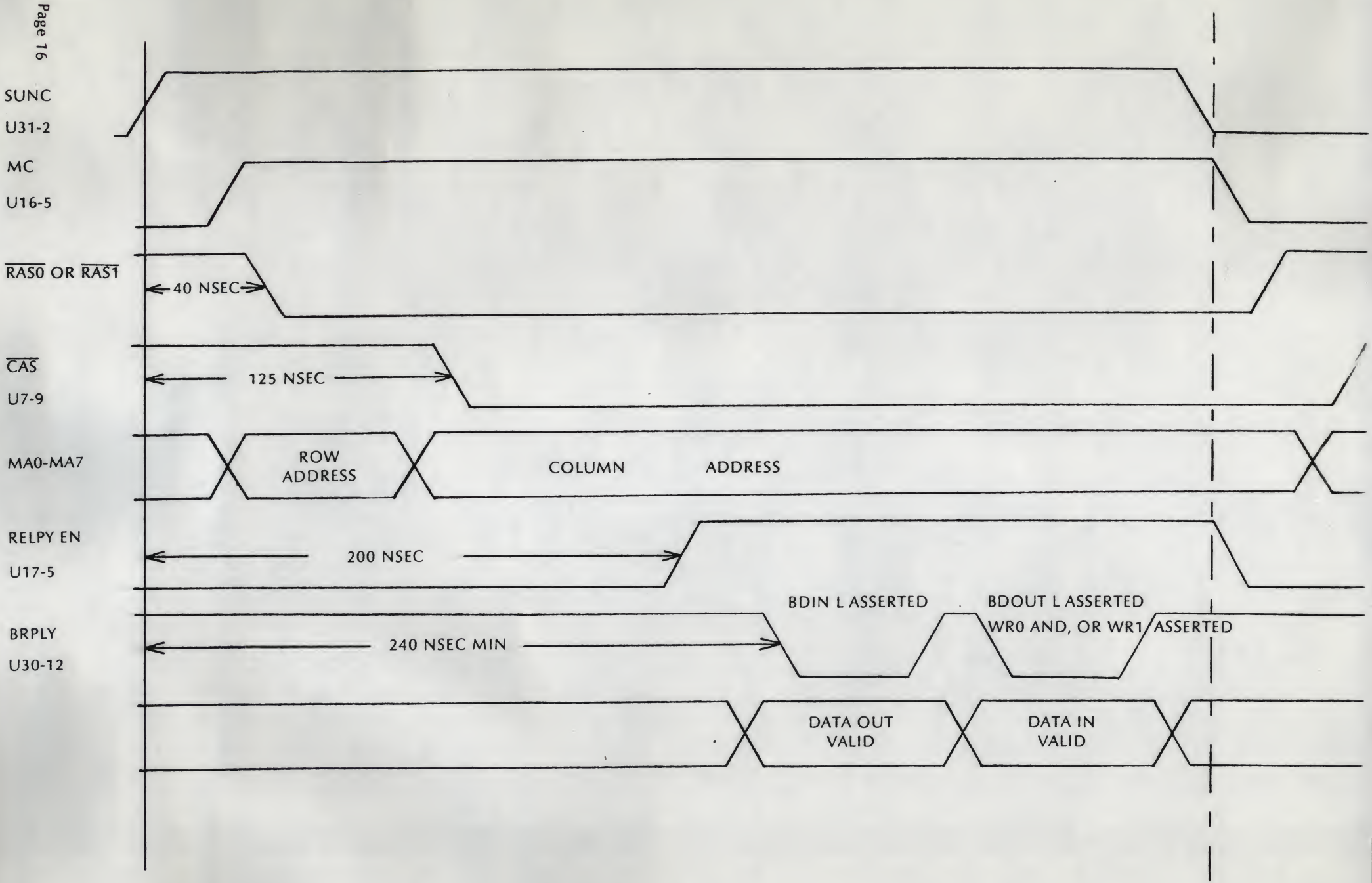


DATA CYCLE TIMING
FIGURE 3.1

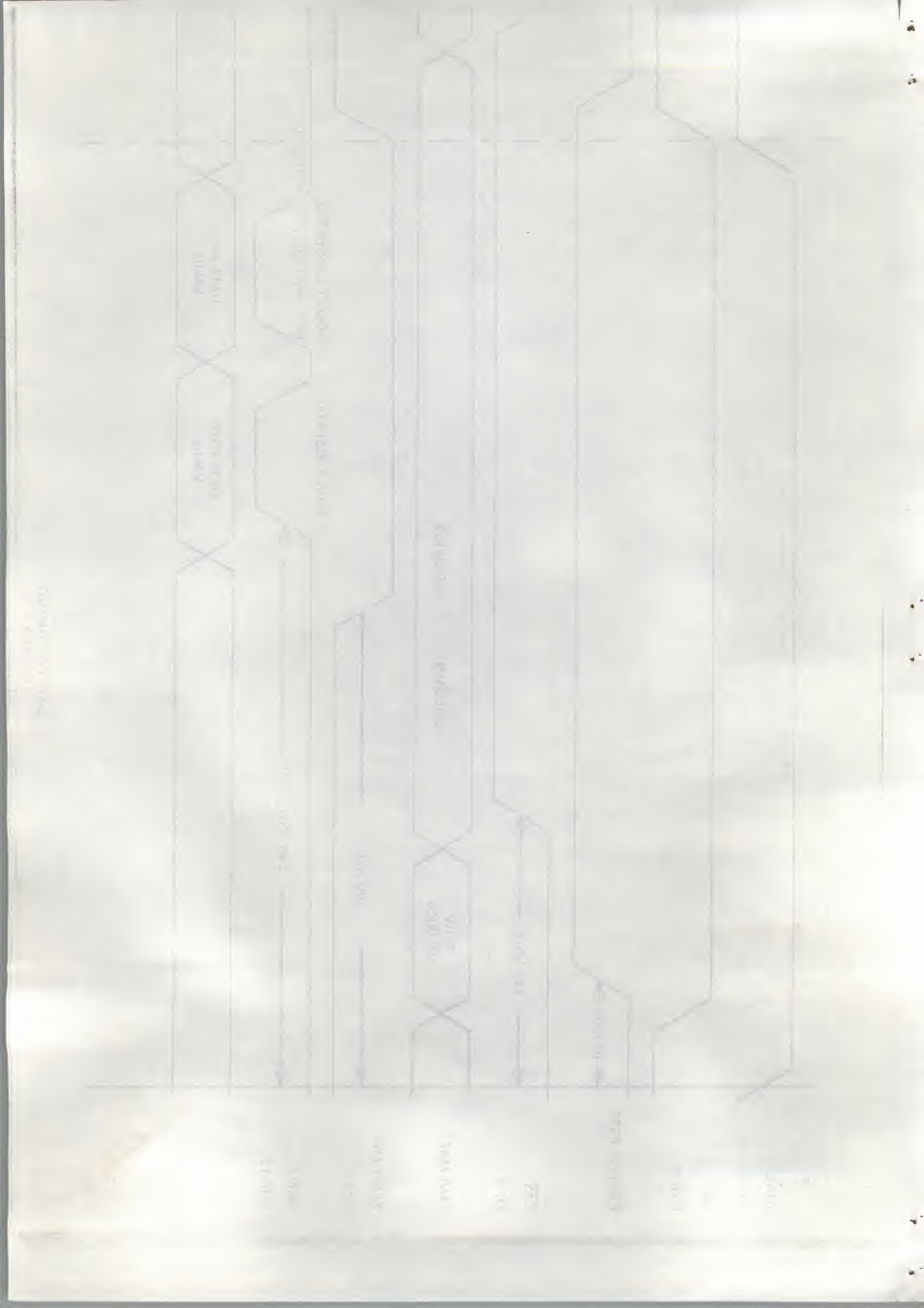


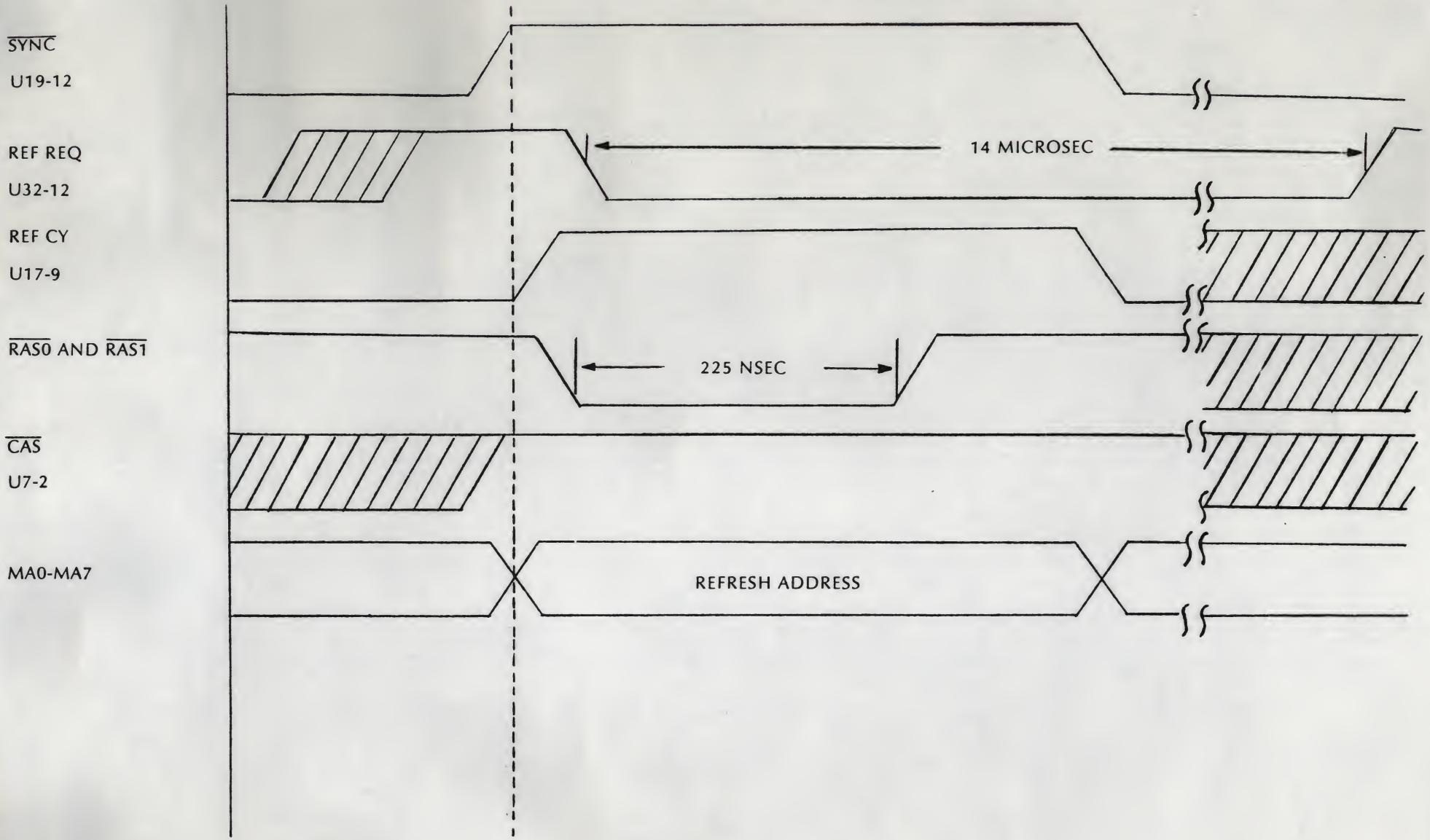


DATO (B) TIMING
FIGURE 3.2

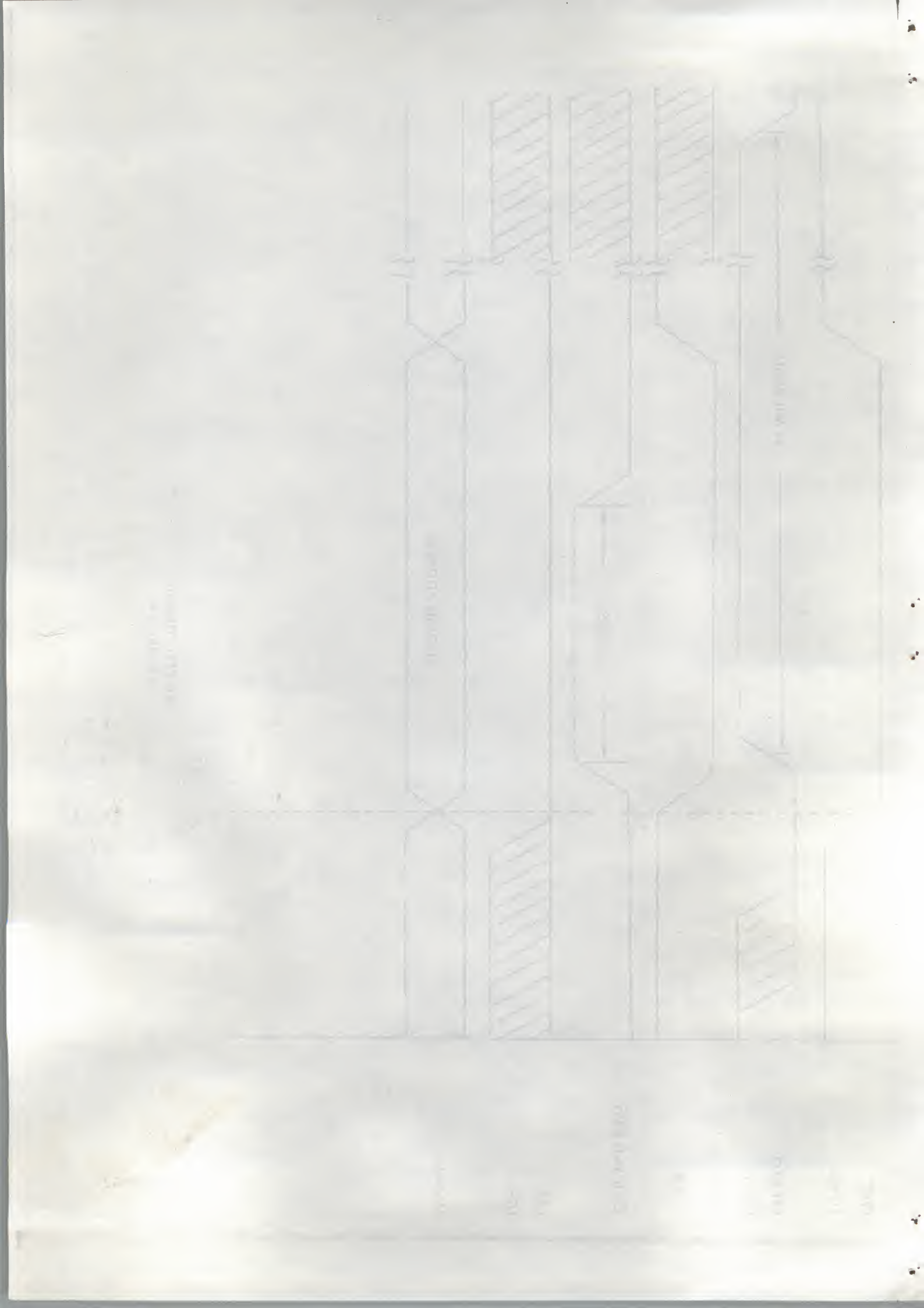


DATIO (B) TIMING
FIGURE 3.3





REFRESH TIMING
FIGURE 3.4



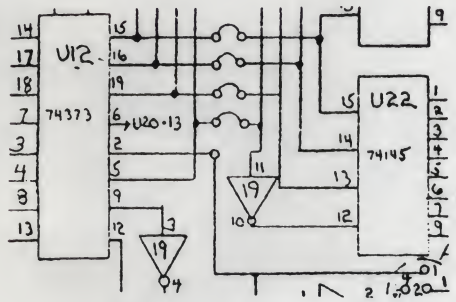
APPENDIX A

MEMORY ADDRESS SELECTION OPTIONS

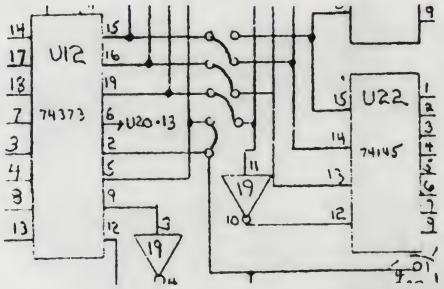
1) RECONFIGURATION FROM OPTION 1 TO OPTION 2

To reconfigure the CI-1123 from 4KW increment selection to 8KW increment selection perform the following:

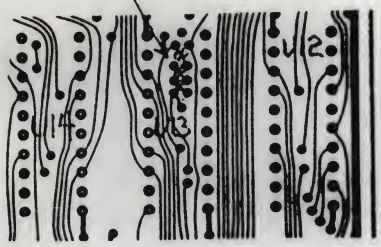
FROM



TO

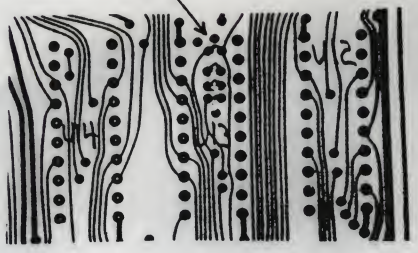


4 ETCH CUTS



SOLDER SIDE

4 JUMPERS



SOLDER SIDE

PEG in AREA A placed between posts 2 and 4.

2) **MEMORY SELECTION IN THE 256K TO 4 MEGABYTE RANGE.**
(Refer to drawing 70754 for location of jumper areas.)

The CI-1123 can be placed in one of sixteen 256K Byte banks from the 0 to 4 megabyte address range. The appropriate 256K Byte is selected according to the following table. Address selection within the bank is according to section 1.4.

TABLE A1-1

BANK SELECTED AREA C PEG POSITION 2 - 3	WIRE-WRAP AREA D	BANK SELECTED AREA C PEG POSITION 2 - 1	WIRE-WRAP AREA D
00000000 to 00777777	1 - 2	10000000 to 10777777	1 - 2
01000000 to 01777777	1 - 3	11000000 to 11777777	1 - 3
02000000 to 02777777	1 - 4	12000000 to 12777777	1 - 4
03000000 to 03777777	1 - 5	13000000 to 13777777	1 - 5
04000000 to 04777777	1 - 6	14000000 to 14777777	1 - 6
05000000 to 05777777	1 - 7	15000000 to 15777777	1 - 7
06000000 to 06777777	1 - 8	16000000 to 16777777	1 - 8
07000000 to 07777777	1 - 9	17000000 to 17777777	1 - 9

NOTE: 1. The CI-1123 is shipped with jumper between posts 1 and 10 in AREA D. This disables the extended memory selection above. The jumper must be removed for implementation of extended memory selection.

APPENDIX B

BATTERY BACKUP OPTION

To implement battery backup option +5VB (AV1) must be jumpered to supply power for essential circuitry on the CI-1123 in the down state.

For proper backup operation the system must contain a DEC power supply with power fail control logic, or the existing system must meet Q Bus specifications for power up and power down sequencing.

For battery backup option perform the following procedure:

Solder Side of Module (see Figure 1)

2 Etch Cuts

Etch cut #1 - Removes system +5 volts from essential circuitry.
Etch cut #2 - Isolates +5VB from system +5 volts.

1 Jumper

Jumper #1 - Jumpers +5VB (AV1) to power bus of memory module.

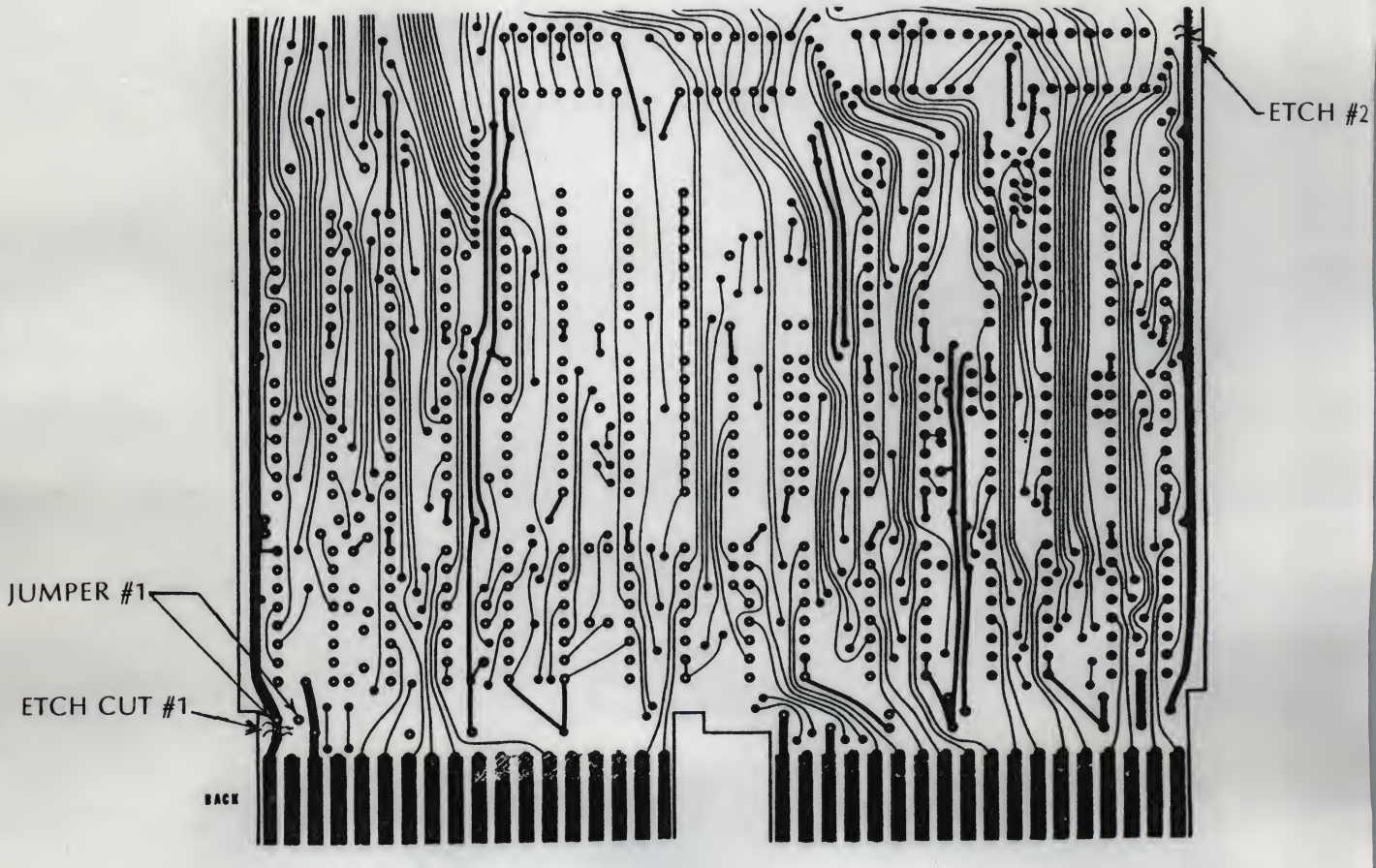


FIGURE #1

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Computer F

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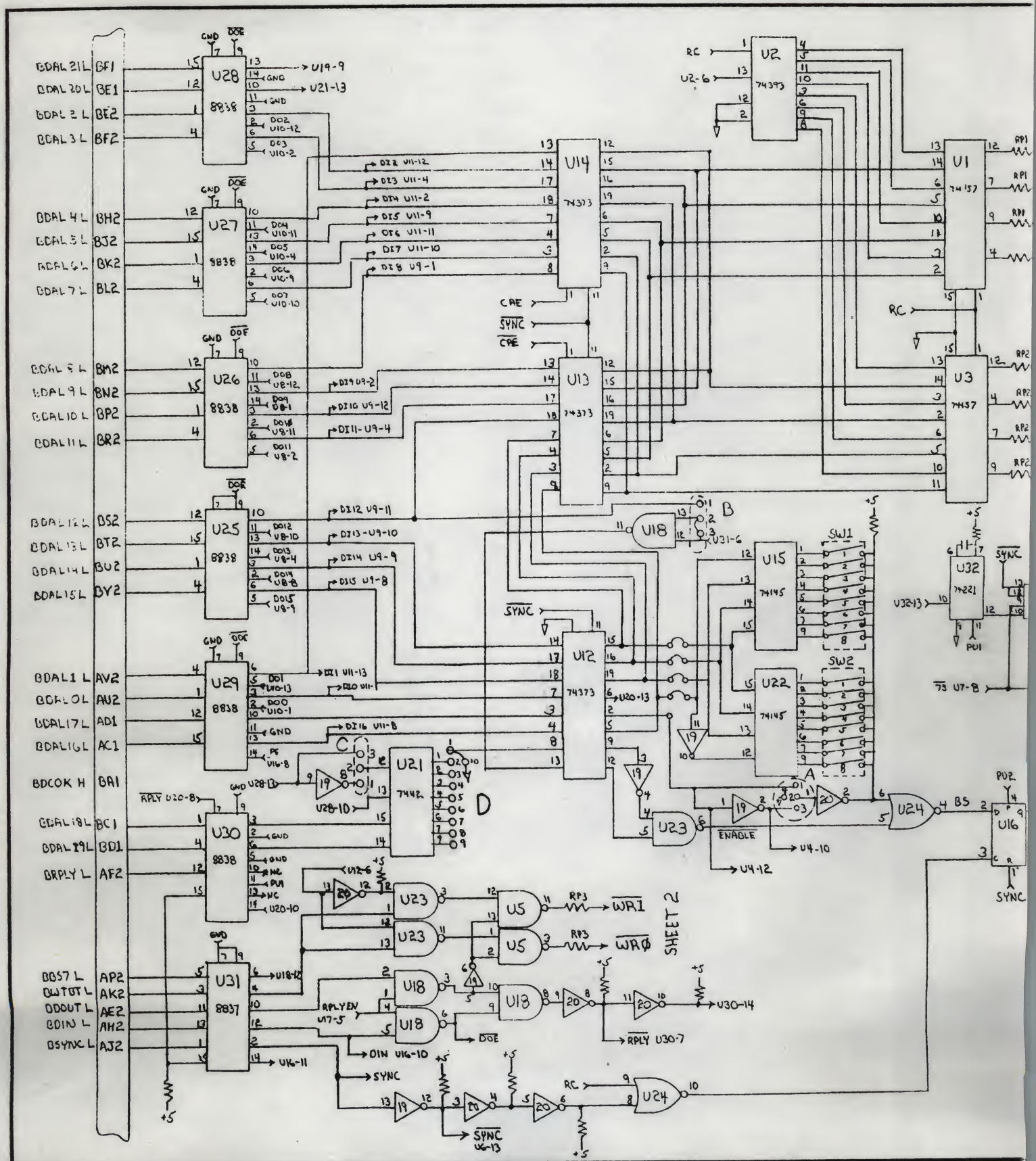
CI-1



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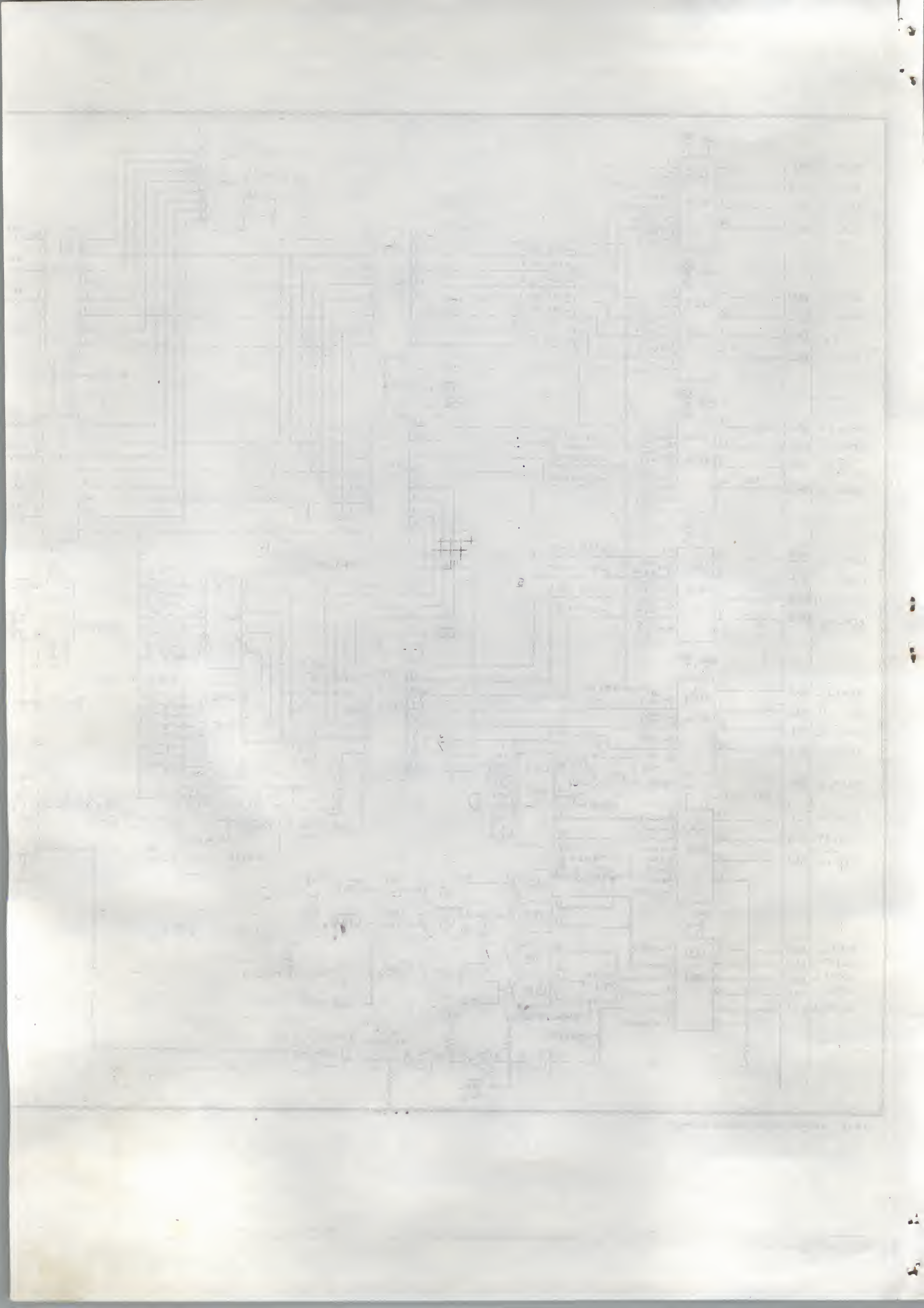

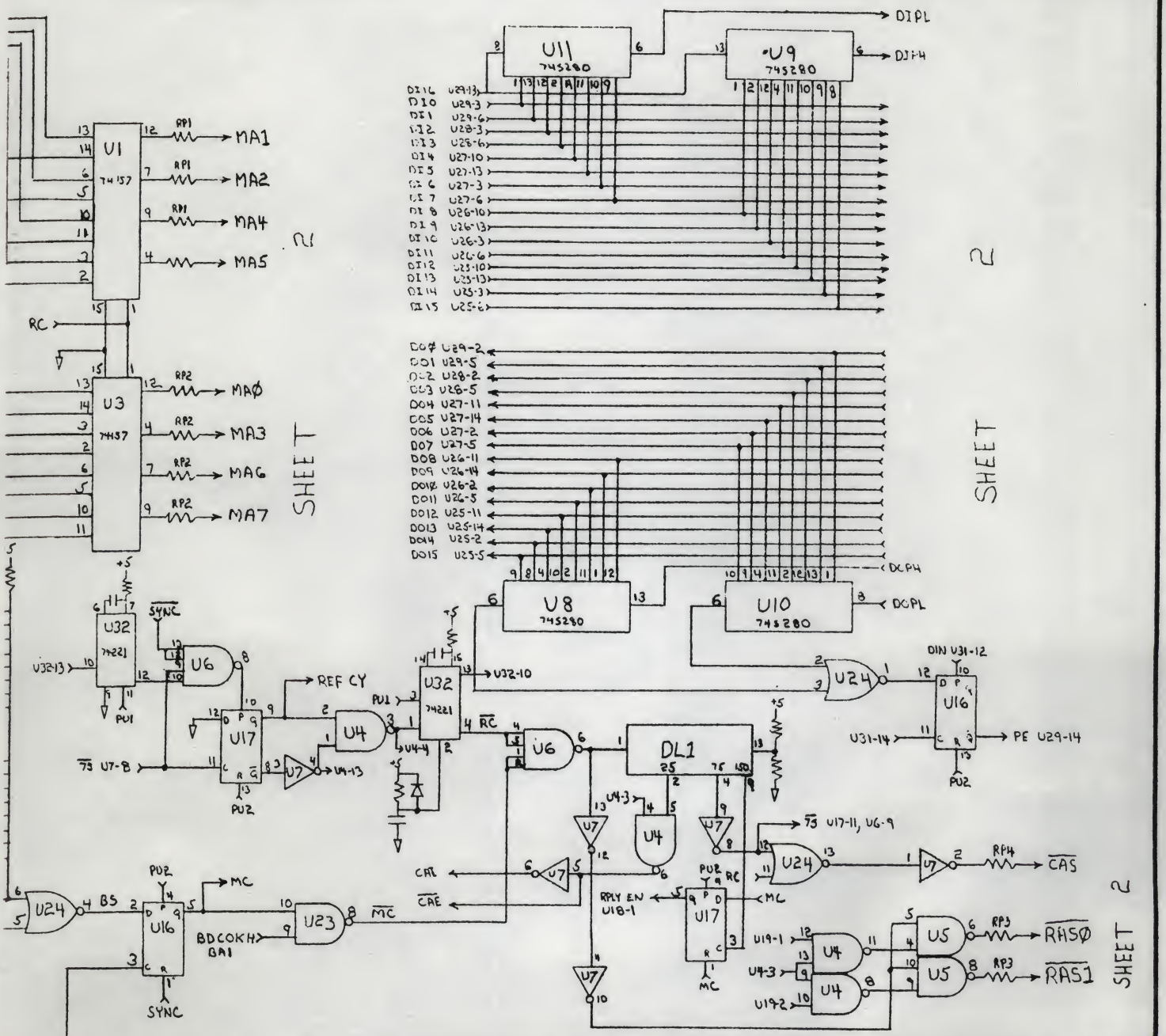

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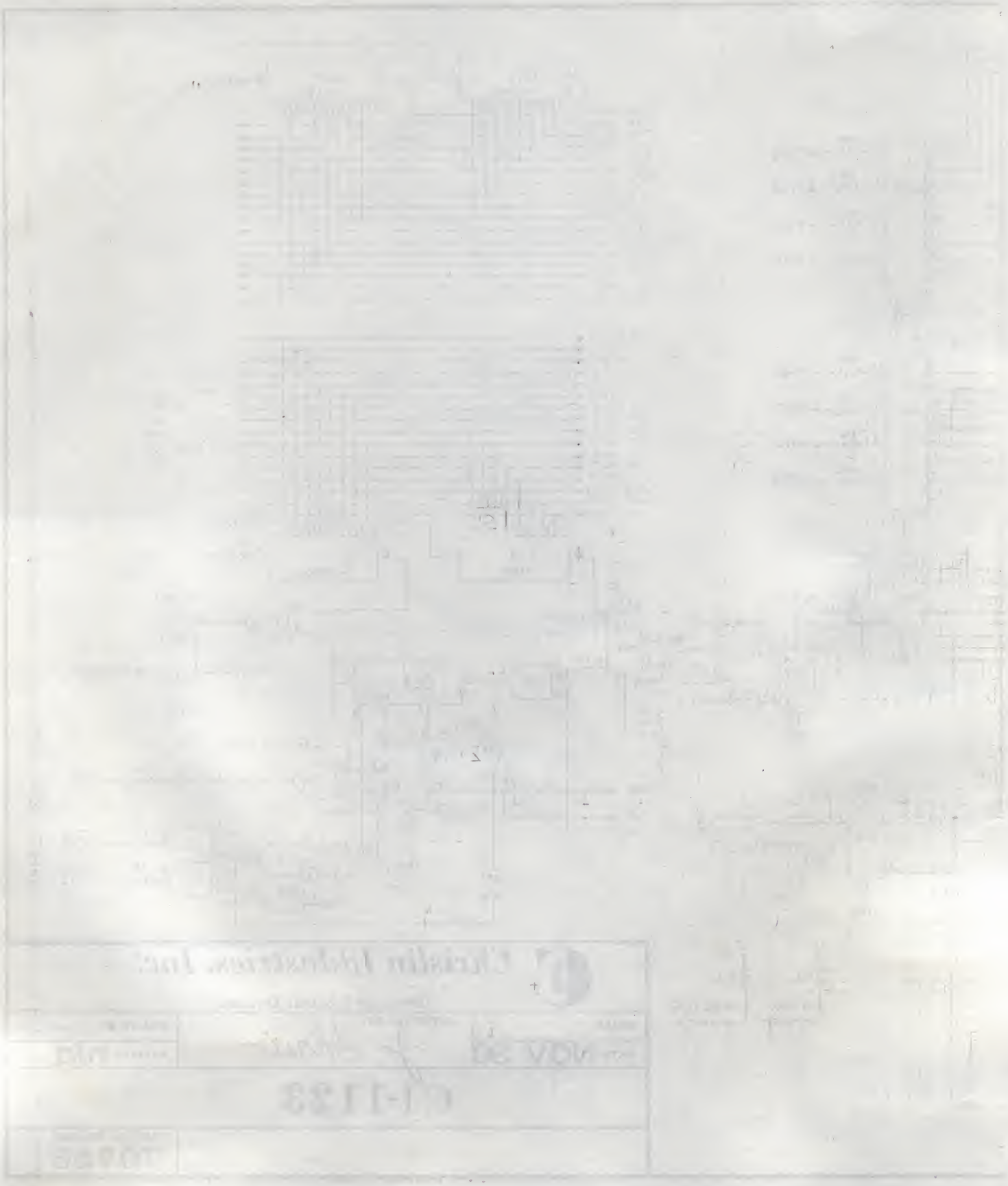

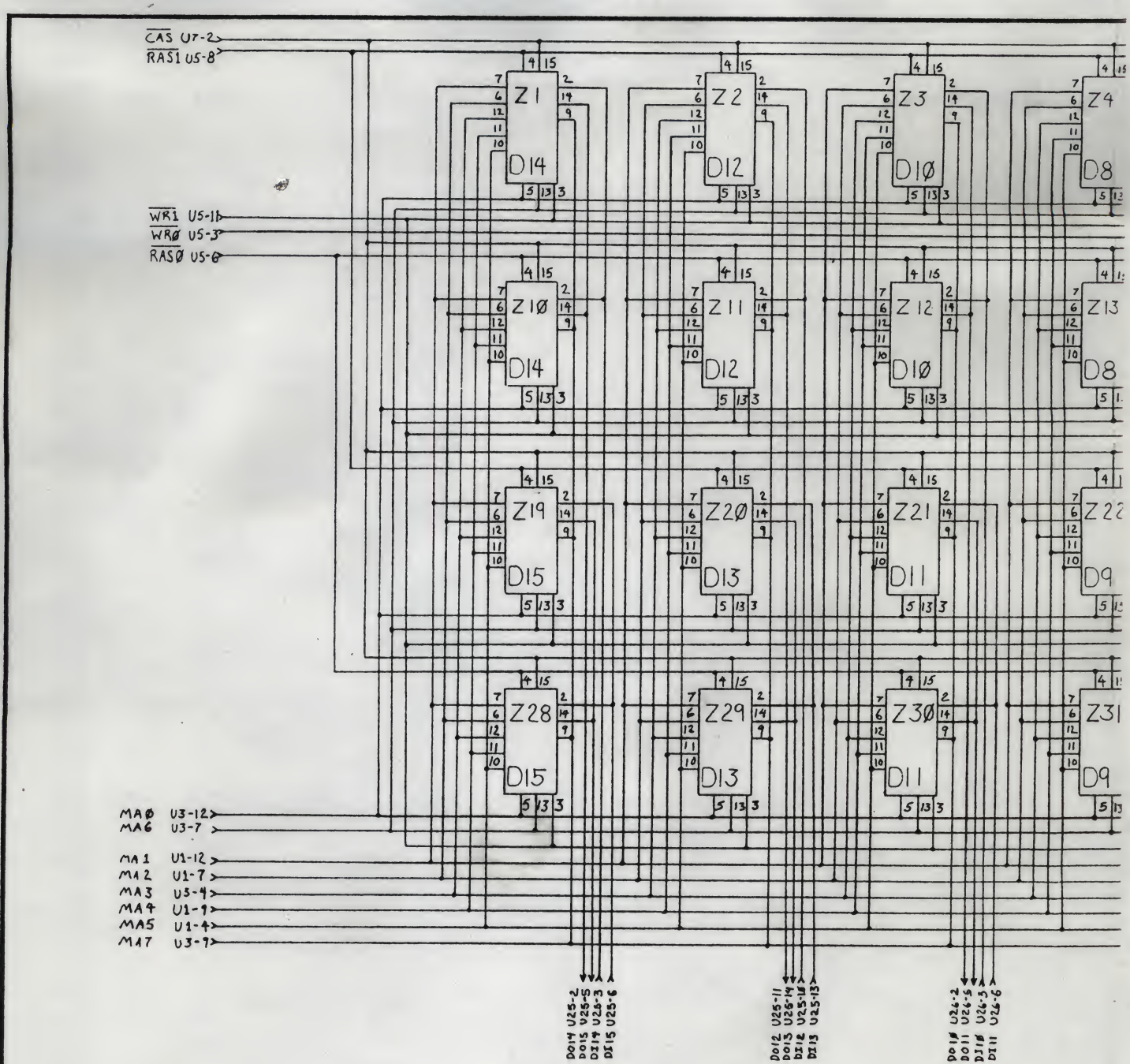
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RAS1 U5-8
WR1 U5-11
WRØ U5-3
RASØ U5-6
Z1
D14
Z2
D12
Z3
D1Ø
Z4
D8
Z1Ø
D14
Z11
D12
Z12
D1Ø
Z13
D8
Z19
D15
Z2Ø
D13
Z21
D11
Z22
D9
Z28
D15
Z29
D13
Z3Ø
D11
Z31
D9
MAØ U3-12
MA6 U3-7
MA1 U1-12
MA2 U1-7
MA3 U3-4
MA4 U1-9
MA5 U1-4
MA7 U3-9
D014 U25-2
D015 U25-5
D114 U26-3
D115 U25-6
D012 U25-11
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D11 U24-5
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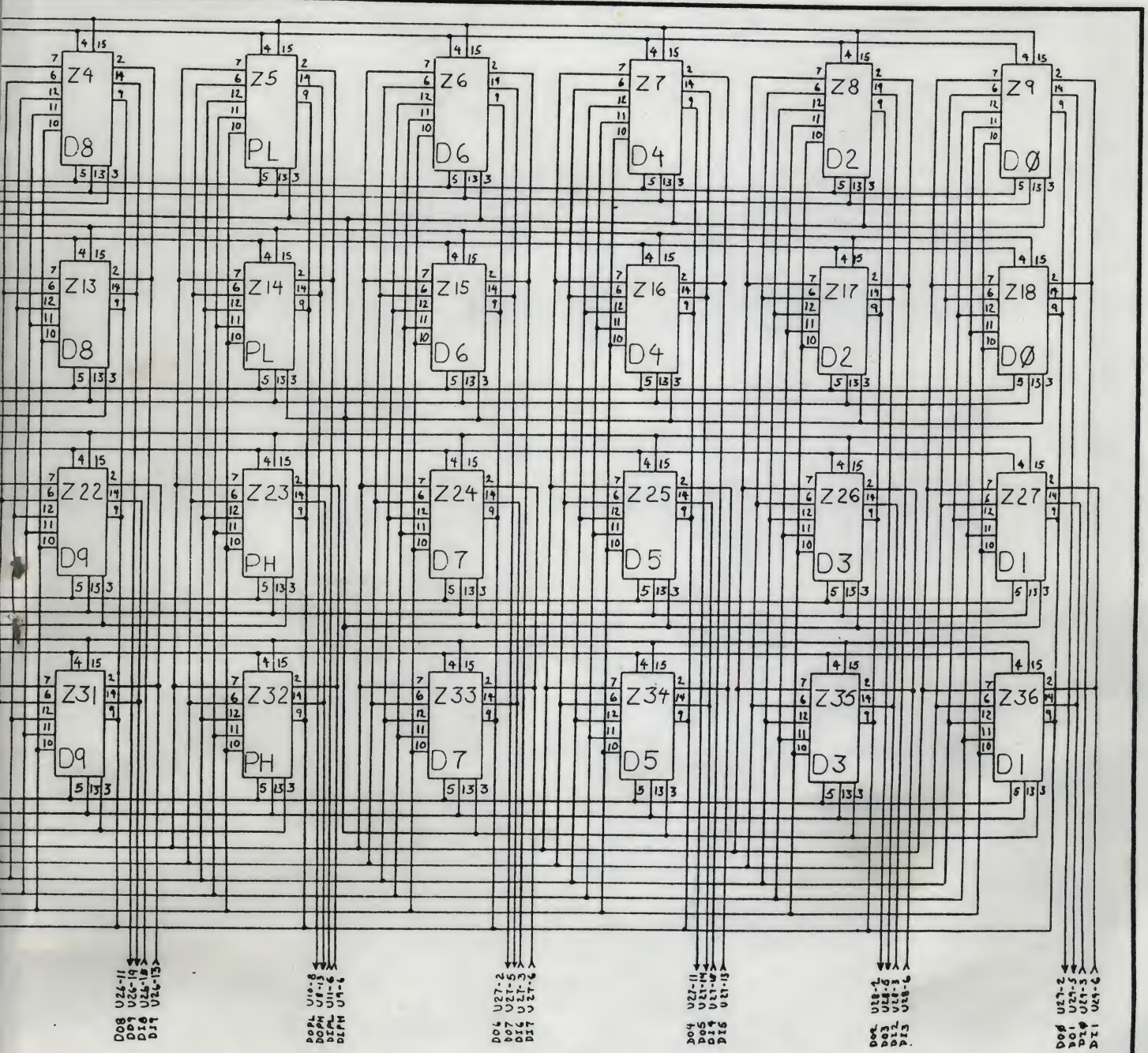
D111 U26-6



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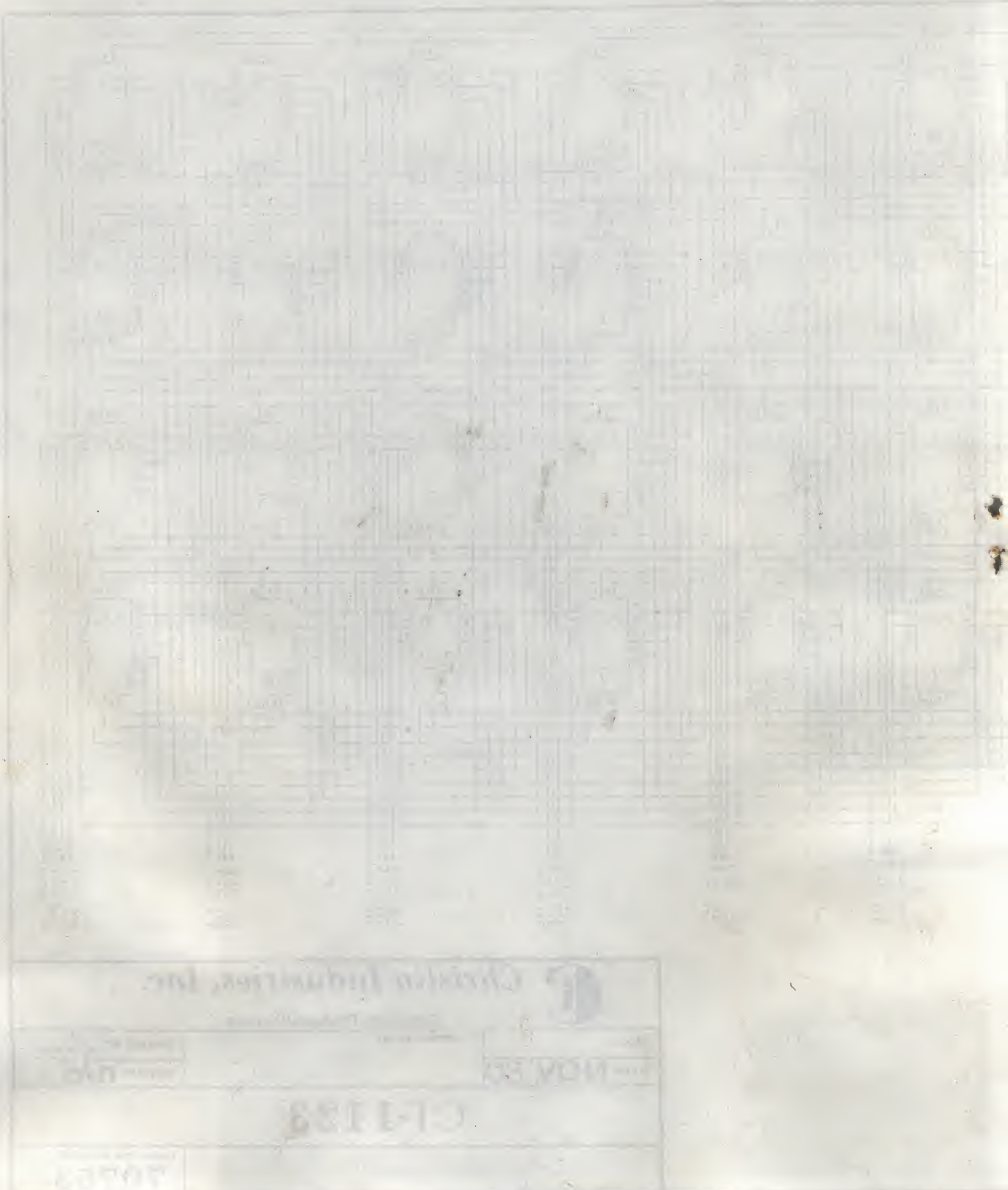
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